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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of)
Michael A. Marra et al.) Group: 2121
Serial No.: 09/226,971)
Filed: January 8, 1999)
Title: METHOD OF REGULATING A TARGET)
SYSTEM USING A FREQUENCY)
COMPARISON OF FEEDBACK AND)
REFERENCE PULSE TRAINS) Examiner: S. R. Garland

SUPPLEMENTAL REPLY BRIEF OF APPELLANT

MS Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Examiner's Supplemental Answer dated September 22, 2004,
Appellants submit the following Supplemental Reply Brief.

This Supplemental Reply does not supplant any of the previous filings by Appellants, but
is proffered for the purpose of responding to the Examiner's Supplemental Answer.

Responsive to the Examiner's argument that claims 1 and 8 of Appellants' invention are
anticipated by U.S. Patent No. 5,212,434 (Hsieh) under 35 U.S.C. § 102(b), Appellants submit
that:

**Appellants reassert that Hsieh does not teach, disclose or suggest the comparison of
frequencies and the generation of a control signal based on that comparison, as recited in
part by claim 1.**

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Please refer to Appellants' Appeal Brief and Reply Brief regarding the background for this assertion. The Examiner indicates that frequencies ω_2 and ω_1 are not the same. Appellants have not implied nor argued that the two signals were the same frequency, rather Appellants have argued that the Appellants' invention generates digital signals in defining a reference pulse train having a frequency dependent upon a reference signal, and compares the frequency of the references pulse train with the frequency of a feed back pulse train and generates a control signal based upon the comparison.

The Examiner has indicated that the meaning of the letters 'PFD' is a phase and frequency detector and then indicates that the comparator has a part number MC4044 as disclosed in the cited IEEE article. Appellants argument includes the assertion that Hsieh discloses only the comparison of the phases of two signals. In the IEEE article, in the second column on page 116, in the paragraph, which starts with the words "Phase Comparator" states:

"it consists of the MC4044 frequency-phase comparator IC and some digital logic gates. R denotes the reference phase and V denotes the variable phase. If R leads V, U will produce pulse outputs and D keeps a high potential. On the other hand, if V leads R, D will produce pulse outputs and U keeps high potential. It is clear from this description of the phase comparator that if the signal R leads or lags signal V that there is a result that changes on outputs D and U."

The D and U outputs are a result of comparing a phase and not a frequency. It is the phase comparison that leads to altering the output signals, and not the generation of a control signal based upon a comparison of frequencies. Nonetheless, even if Hsieh did disclose a comparison of frequencies it does not disclose the generation of a plurality of digital signals defining a reference pulse train with a frequency dependent upon a reference signal, comparing the reference pulse train to a feed back pulse train and utilizing that comparison to generate a control

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signal, as claimed by Appellants' in claim 1.

The advantages of Appellants' invention over Hsieh include simplicity of design having fewer circuit elements with less space required for the control mechanism. This is a partial result of Appellants' invention not detecting nor correcting any phase differences between a reference signal and a feed back signal thereby resulting in the reduced circuitry and cost of Appellants' invention.

For all of the foregoing reasons, Appellants submit that claims 1 and 8, are in condition for allowance, the allowance of which is hereby respectfully requested.

Responsive to the Examiner's argument that Claims 2, 3 and 5 of Appellants' invention are unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan) under 35 U.S.C. § 103(a), Appellants submit that:

The references, taken alone or in combination, fail to teach, disclose or suggest, alone or in combination, the comparison of frequencies, the generation of a control signal based on that comparison and substantially aligning a leading edge of each digital signal in the reference pulse train with a leading edge of the feedback signal, as recited in part by claim 2.

Please refer to Appellants' Appeal Brief and Reply Brief regarding the background for this assertion.

The Examiner at page 6 of the Supplemental Examiner's Answer indicates that, "it would have been obvious to one of ordinary skill in the art to modify Hsieh in view of Long or O'Sullivan and use the leading edges for ease in determining the phase error." First, Appellants',

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invention does not determine any phase errors, rather it is directed toward the frequency of two signals. Second, the use of leading edges for the ease of determining phase error is not on point with what Appellants' invention, as recited in claim 2, claims. Claim 2 includes the limitation of substantially aligning a leading edge of each digital signal in the reference pulse train with a leading edge of the digital signal in the feedback pulse train. In Appellants' invention the signals are actively aligned to assist in the generation of a control signal. The alignment is not part of minimizing the phase between the signals. It is the difference between each pair of aligned pulses that is used to generate a proportional error pulse train having a plurality of digital signals (Application, page 8, lines 18-23). The internal alignment of the pulse trains within Appellants' invention is not used to determine any phase error as suggested by the Examiner.

The advantages of Appellants' invention over Hsieh include simplicity of design and having fewer circuit elements in less space. This is a partial result of Appellants' invention not detecting nor correcting any phase differences between a reference signal and a feedback signal thereby resulting in the reduced circuitry and cost of Appellants' implementation.

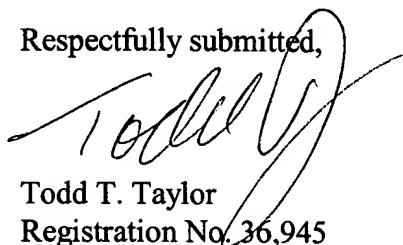
For all of the foregoing reasons, Appellants submit that claim 2, and claims 3 and 5 depending therefrom, are in condition for allowance, the allowance of which is hereby respectfully requested.

For the foregoing reasons, Appellants submit that claims 1-3, 5 and 8 are neither anticipated nor suggested by the cited references, alone or in combination, and are therefore in

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condition for allowance in their present form. Accordingly, Appellants respectfully request the Board to reverse the final rejections of the appealed claims.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF Commissioner for Patents, Washington, DC 20231, on: November 22, 2004

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Signature
November 22, 2004

Date